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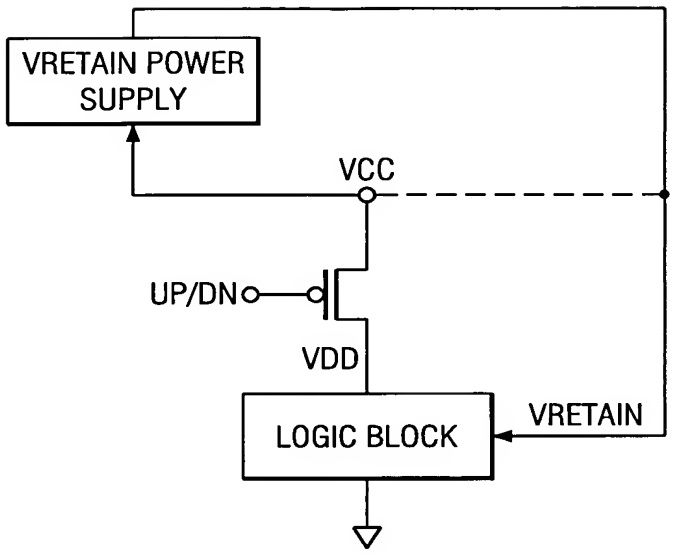

FIG. 1

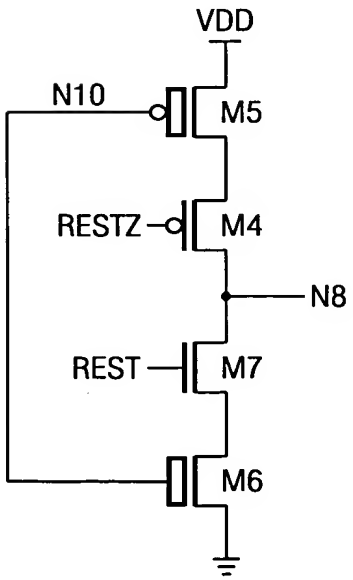

FIG. 3

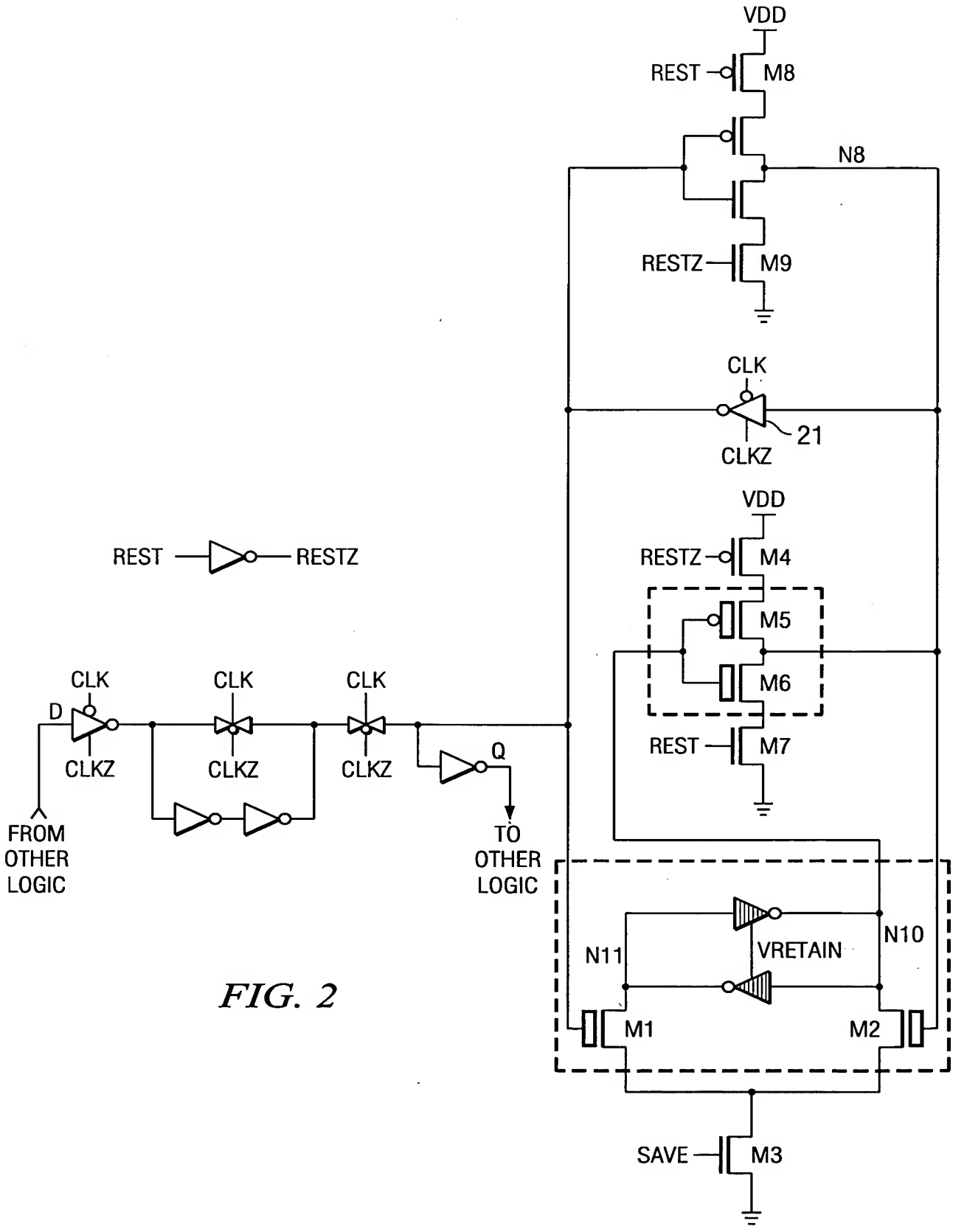
VDD
REST
M8
N8
RESTZ
M9
CLK
21
CLKZ
VDD
REST
RESTZ
RESTZ
M4
M5
M6
CLK
CLK
CLK
D
REST
M7
CLKZ
CLKZ
CLKZ
Q
FROM
OTHER
LOGIC
TO
OTHER
LOGIC
N11
VRETAIN
N10
M1
M2
SAVE
M3

FIG. 2

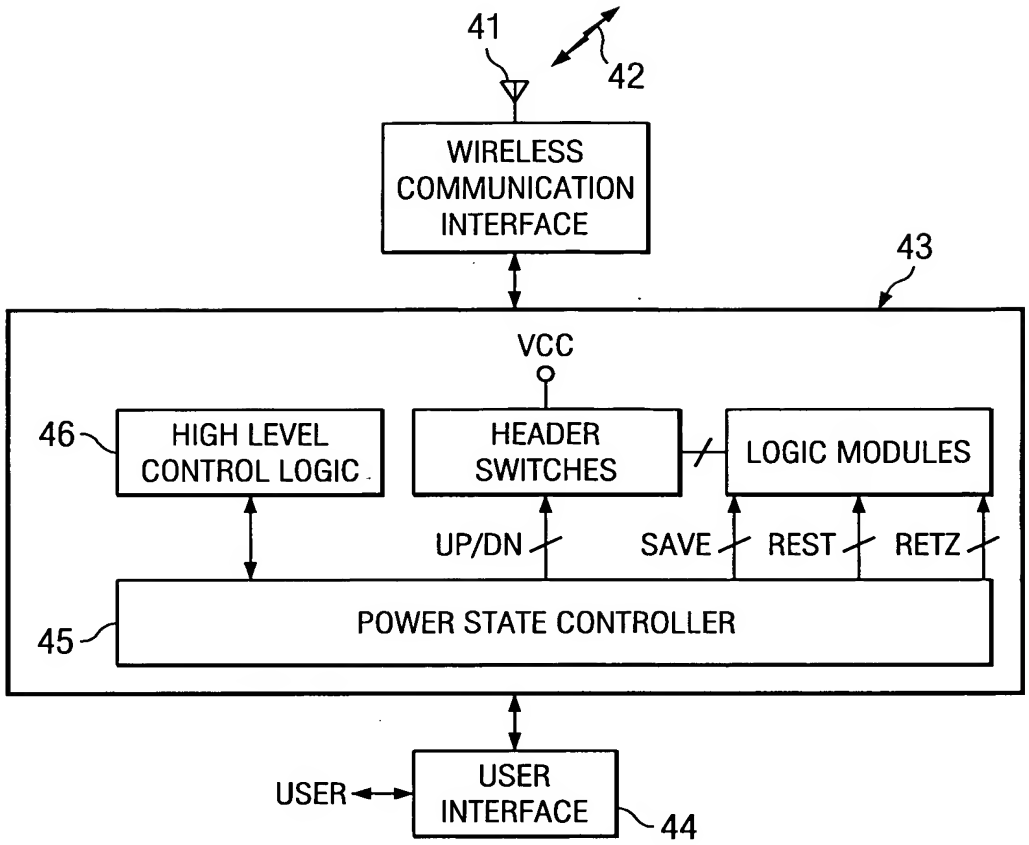
41
42
WIRELESS COMMUNICATION INTERFACE
43
VCC
46
HIGH LEVEL CONTROL LOGIC
HEADER SWITCHES
LOGIC MODULES
UP/DN
SAVE
REST
RETZ
45
POWER STATE CONTROLLER
USER
USER INTERFACE
44

FIG. 4

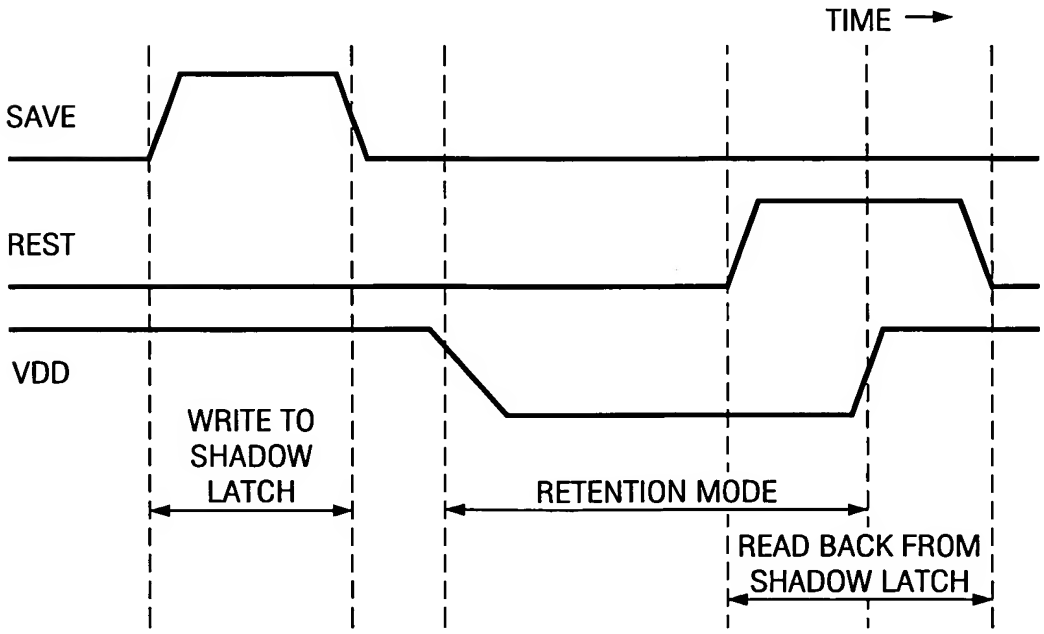
TIME
SAVE
REST
VDD
WRITE TO SHADOW LATCH
RETENTION MODE
READ BACK FROM SHADOW LATCH

FIG. 5

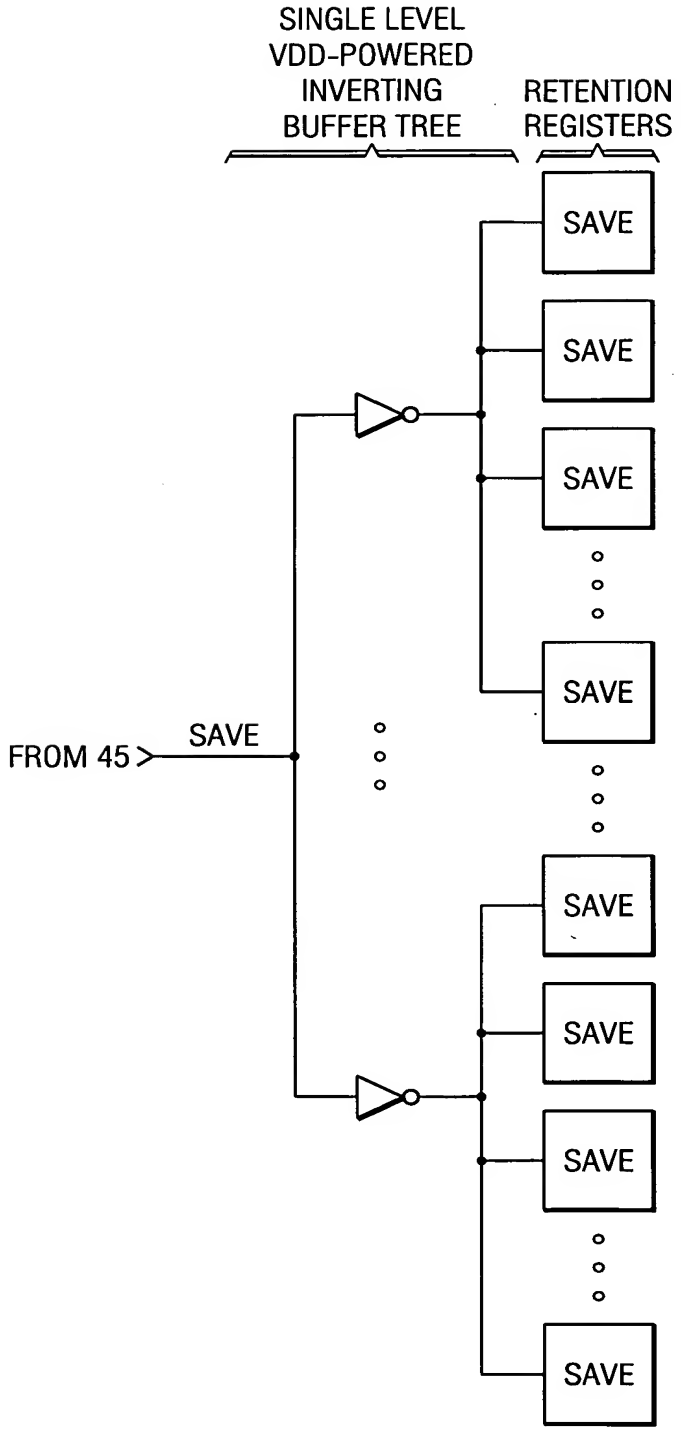
SINGLE LEVEL
VDD-POWERED
INVERTING
BUFFER TREE
RETENTION
REGISTERS
SAVE
SAVE
SAVE
SAVE
FROM 45
SAVE
SAVE
SAVE
SAVE
SAVE

FIG. 6

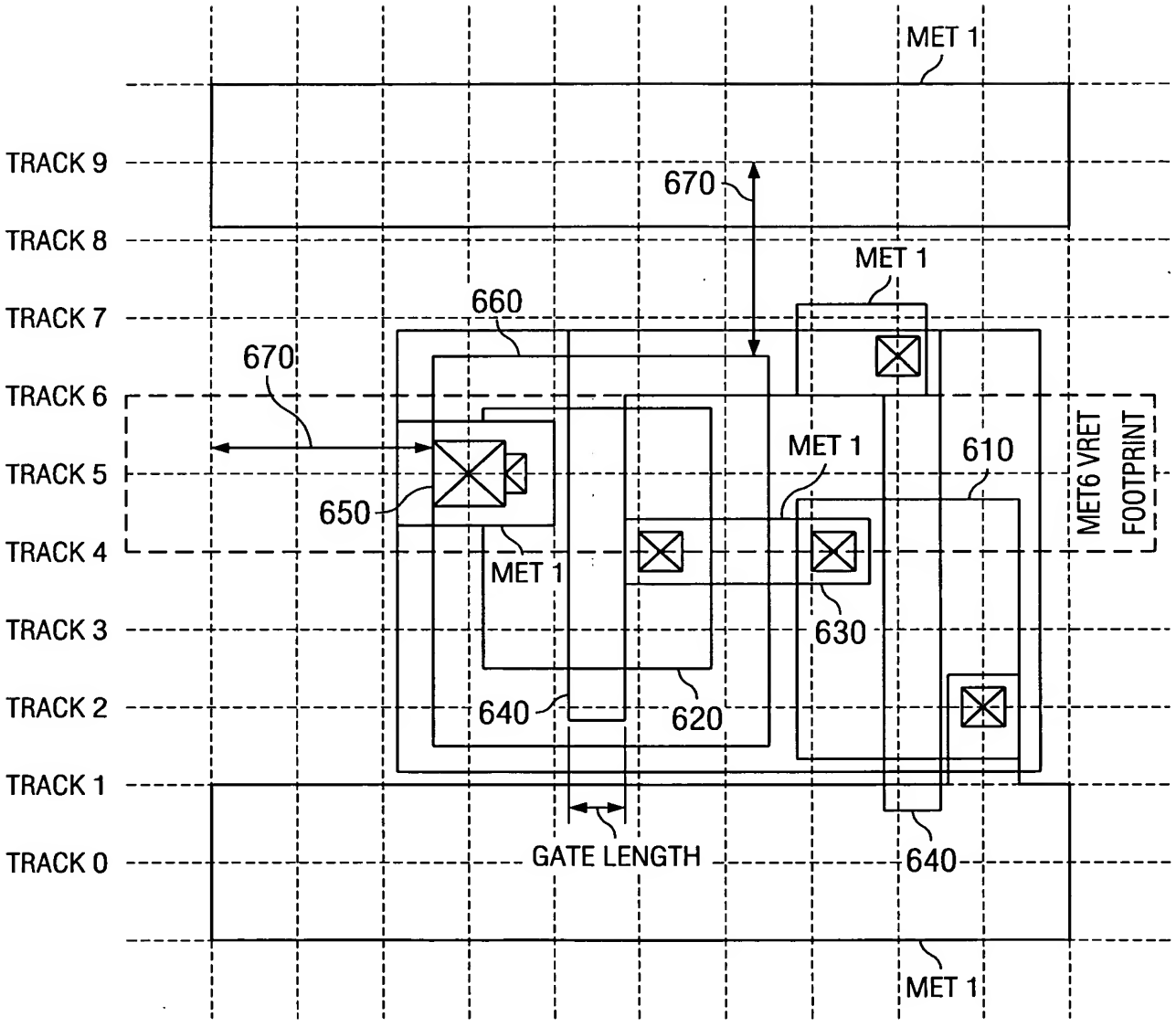
MET 1
TRACK 9
670
TRACK 8
MET 1
TRACK 7
660
670
TRACK 6
MET 1
610
MET6 VRET
FOOTPRINT
TRACK 5
650
TRACK 4
MET 1
630
TRACK 3
640
620
TRACK 2
TRACK 1
GATE LENGTH
640
TRACK 0
MET 1

FIG. 6A

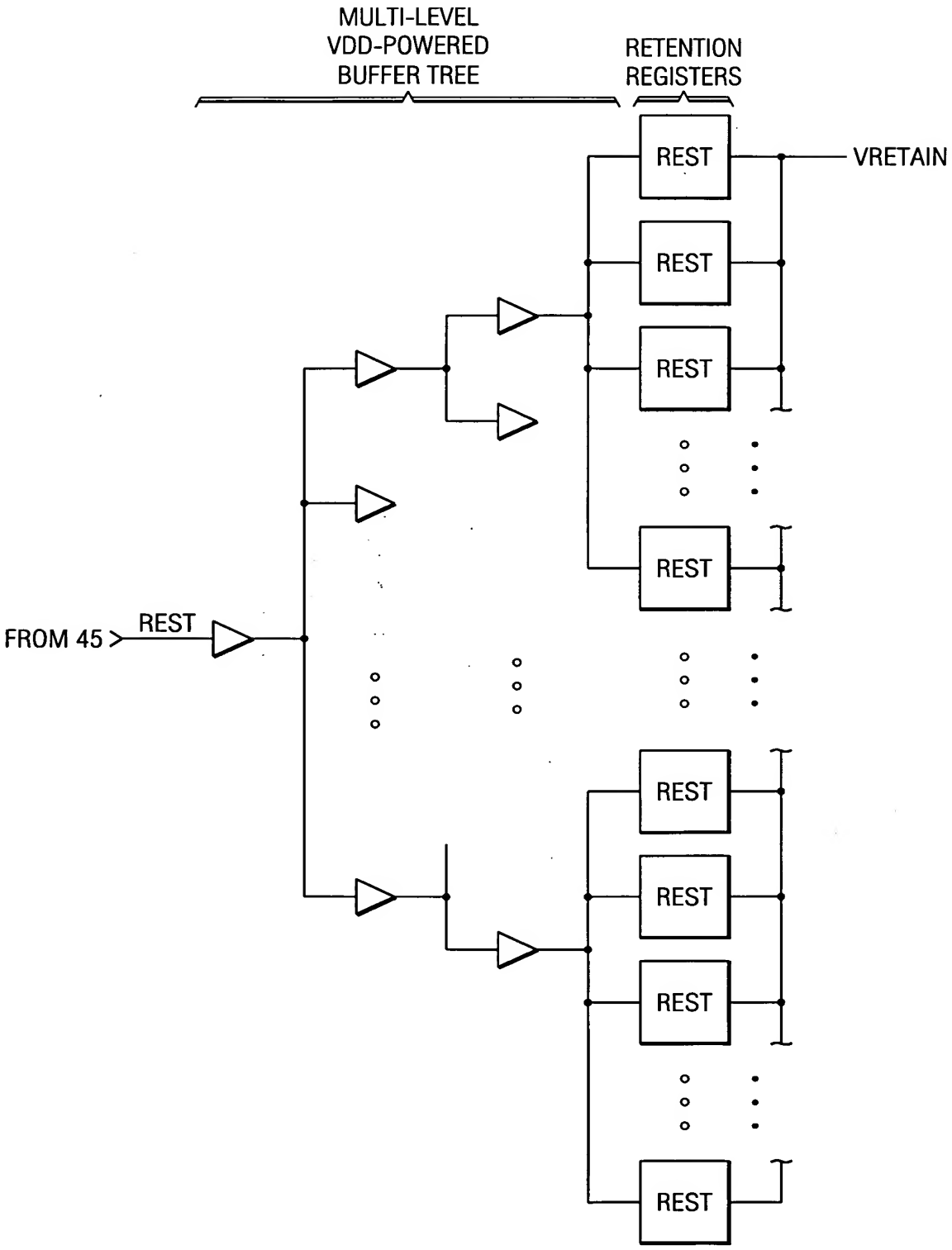
MULTI-LEVEL
VDD-POWERED
BUFFER TREE
RETENTION
REGISTERS
REST
VRETAIN
REST
REST
REST
FROM 45
REST
REST
REST
REST
REST
REST

FIG. 7

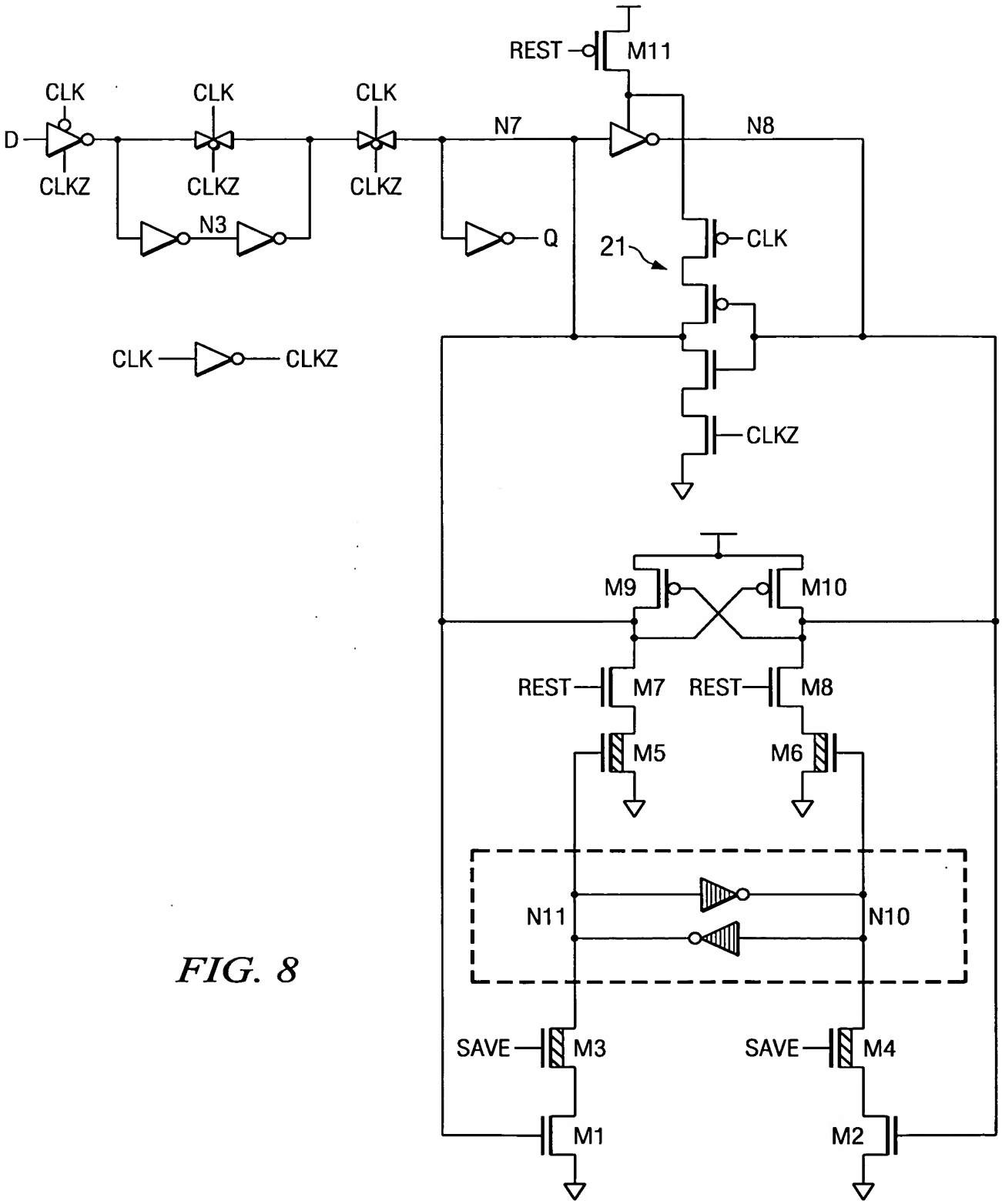
REST
M11
CLK
CLK
CLK
D
N7
N8
CLKZ
CLKZ
CLKZ
N3
Q
21
CLK
CLK
CLKZ
CLKZ
M9
M10
REST
M7
REST
M8
M5
M6
N11
N10
SAVE
M3
SAVE
M4
M1
M2

FIG. 8

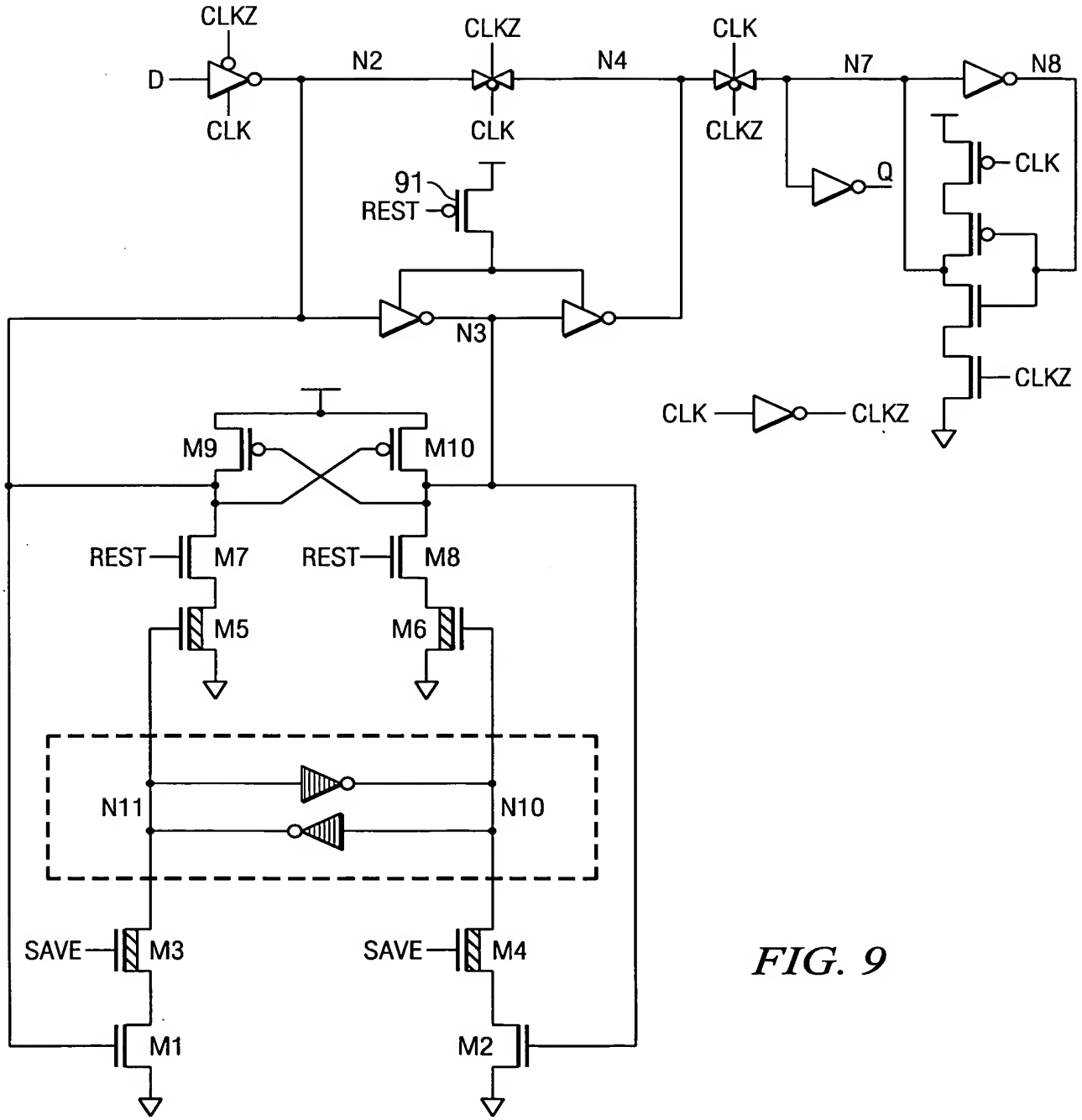
CLKZ
D
CLK
N2
CLKZ
CLK
N4
CLK
CLKZ
N7
N8
Q
CLK
91
REST
N3
CLKZ
CLK
CLKZ
M9
M10
REST
M7
REST
M8
M5
M6
N11
N10
SAVE
M3
SAVE
M4
M1
M2

FIG. 9

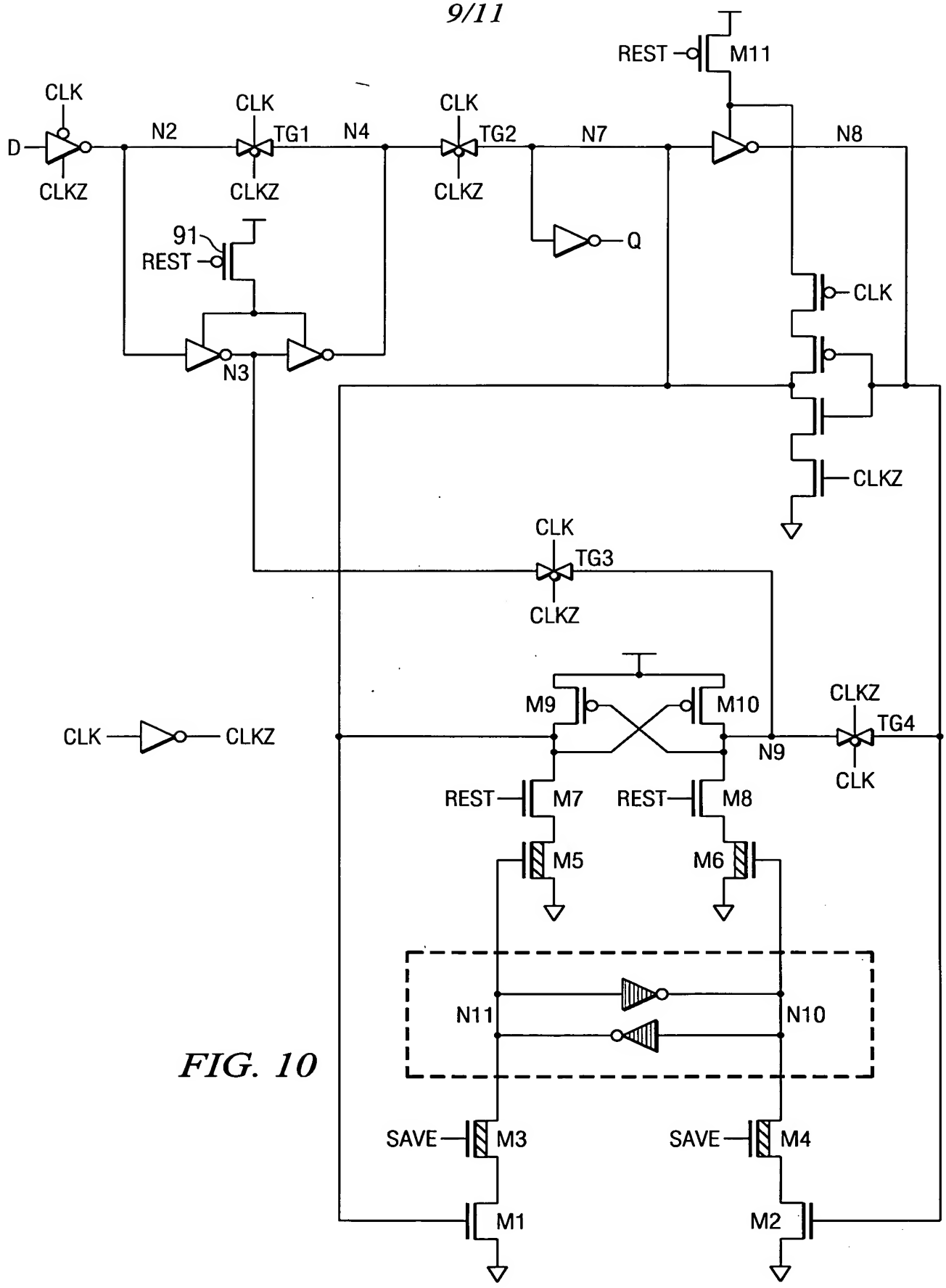
REST
M11
CLK
D
CLKZ
N2
CLK
TG1
CLKZ
N4
CLK
TG2
CLKZ
N7
N8
91
REST
Q
CLK
N3
CLKZ
CLK
TG3
CLKZ
CLK
CLKZ
M9
M10
CLKZ
TG4
N9
CLK
REST
M7
REST
M8
M5
M6
N11
N10
SAVE
M3
SAVE
M4
M1
M2

FIG. 10

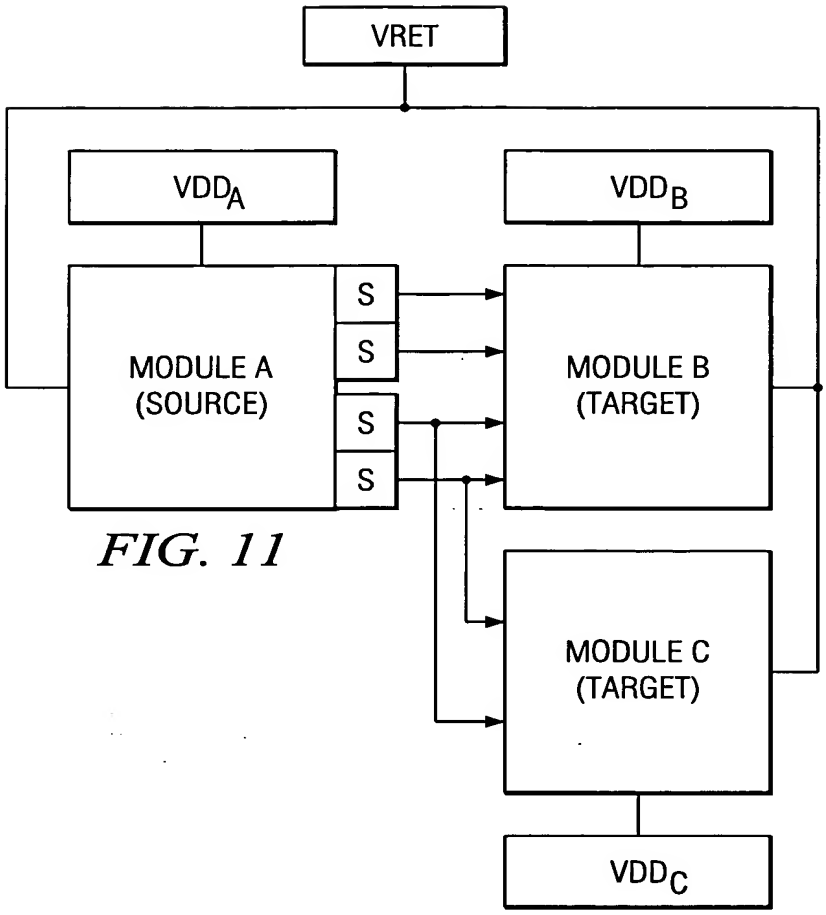
VRET
VDD$_A$
VDD$_B$
MODULE A
(SOURCE)
S
S
S
S
MODULE B
(TARGET)
MODULE C
(TARGET)
VDD$_C$

FIG. 11

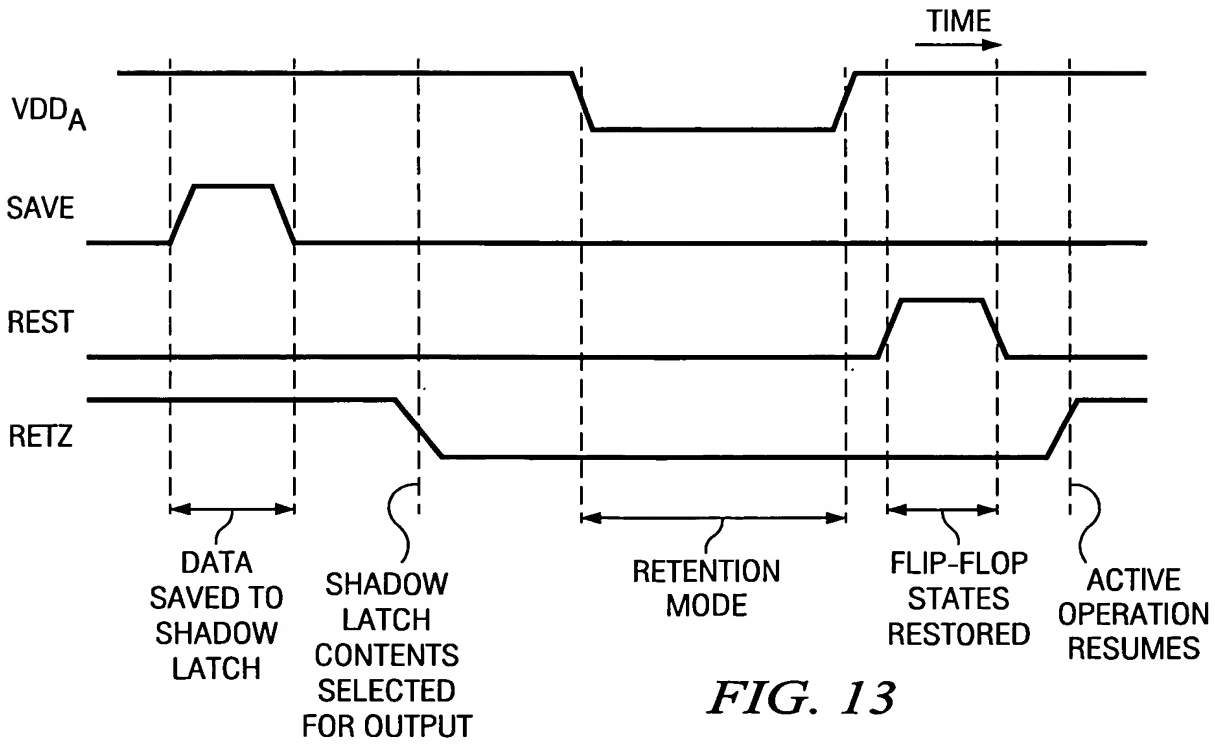
TIME
VDD$_A$
SAVE
REST
RETZ
DATA SAVED TO SHADOW LATCH
SHADOW LATCH CONTENTS SELECTED FOR OUTPUT
RETENTION MODE
FLIP-FLOP STATES RESTORED
ACTIVE OPERATION RESUMES

FIG. 13

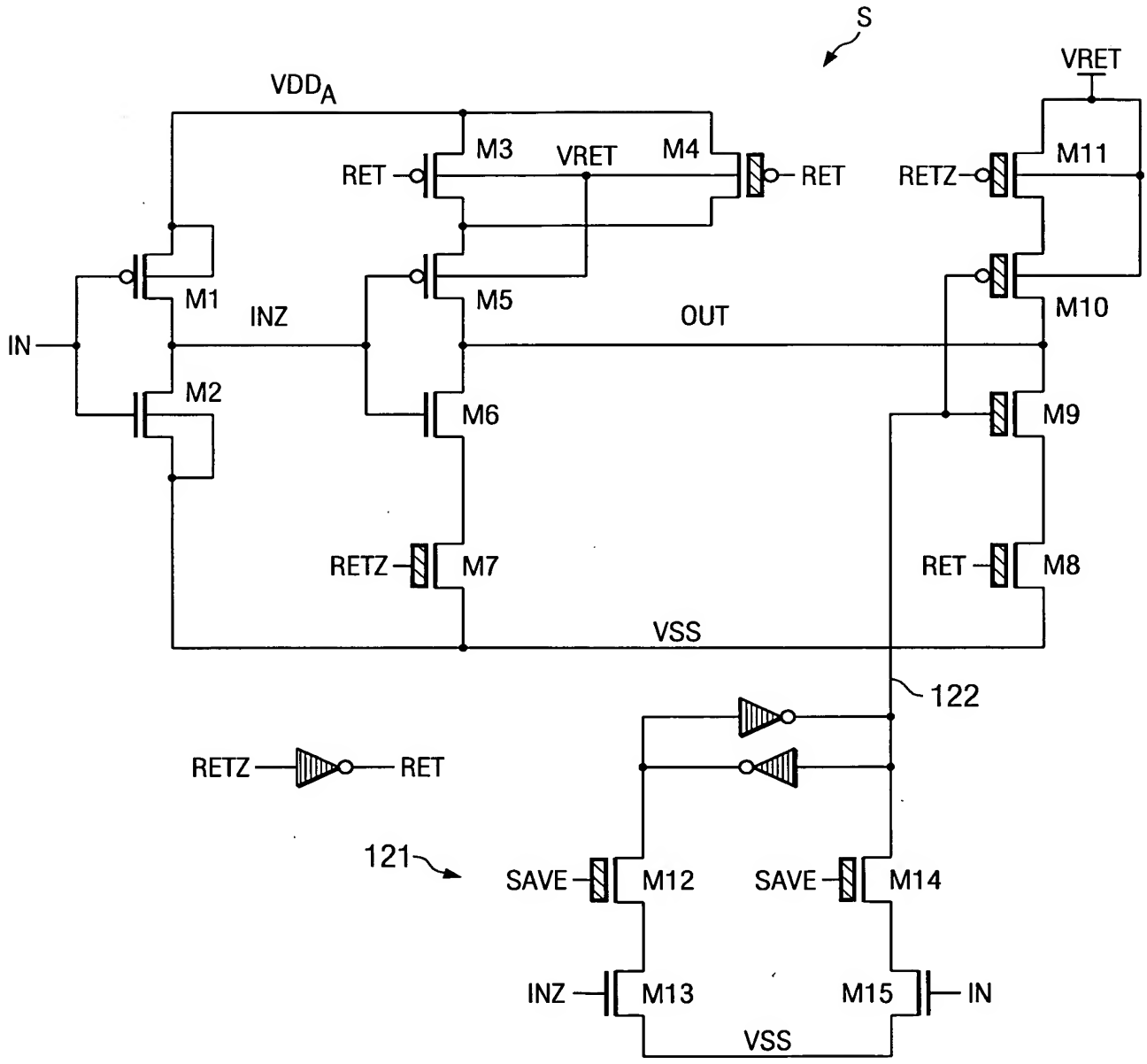
S
VRET
VDD$_A$
M3
VRET
M4
RET
RET
RETZ
M11
M1
M5
M10
IN
INZ
OUT
M2
M6
M9
RETZ
M7
RET
M8
VSS
122
RETZ
RET
121
SAVE
M12
SAVE
M14
INZ
M13
M15
IN
VSS

FIG. 12